

Synopsis V1.0
SEE Test Report for the Samsung DDR DRAM

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I. Introduction

This study was undertaken to determine the susceptibility of the Samsung KH41G0X38 1 Gbit DDR DRAM to destructive and nondestructive single-event effects (SEE). The device was monitored for SEUs, functional interrupts and destructive events induced by exposing it to a heavy ion beam at Michigan State University's SEE Test Facility. Subsequent heavy-ion testing was done at the Texas A&M University (TAMU) Cyclotron Institute, and proton testing was done at the Indiana University Cyclotron Facility (IUCF).

II. Devices Tested

We tested a single Samsung KH41G0X38 DRAMs marked with date code 0546. Note that with commercial devices, the same lot date code is no guarantee that the devices are from the same wafer diffusion lot or even from the same fabrication facility. However, we believe that since these devices are fabricated in the still relatively rare 90 nm feature-size technology and were supplied by the manufacturer that their provenance is traceable.

The device technology is 90 nm minimum feature size CMOS Double-Data-Rate Synchronous Dynamic Random Access Memory.

III. Test Facility

Facilities: SEETF at the National Superconducting Cyclotron Facility (NSCL), Michigan State University (MSU)

Texas A&M University (TAMU)

Indiana University Cyclotron Facility (IUCF)

Flux: $(5 \times 10^2 \text{ to } 1. \times 10^5 \text{ particles/cm}^2/\text{s})$.

Fluence: All heavy-ion tests were run to $(1 \times 10^6 \text{ p/cm}^2)$ or until destructive or functional events occurred. Proton irradiations were conducted to a fluence of $8.37 \times 10^{10} \text{ particles/cm}^2$.

Table I: Ions/Energies and LET for this test

Ion	Energy/AMU	Angle	Facility	Effective LET	Residual Range
Xe-136	69.9	0	NSCL	27	640 μm
Xe-136	69.9	45	NSCL	46.5	182 μm
Xe-136	69.9	60	NSCL	108	123 μm
Ne-20	40	0	TAMU	1.4	1100 μm
Ar-40	40	0	TAMU	5.8	420 μm
Proton	200	Various	IUCF	N/A	Not a factor

Test Conditions

Test Temperature: Room Temperature for SEU, 85°C

Operating Frequency: (0-100 MHz).

Power Supply Voltage: (2.5V for both SEL SEU).

IV. Test Methods

Because of the mode of operation of DRAM, all testing was performed dynamically at a clock speed of 100 MHz (DDR speed of 200 MHz) and with a checkerboard pattern (AA).

The Block diagram for control of the DUT is shown in Figure 1. The FPGA based controller interfaces to the FLASH daughter card and to a laptop, allowing control of the FPGA and uploading of new FPGA configurations and instructions for control of the DUT. Power for the DUT is supplied by means of a computer-controlled power supply. The National Instruments Labview interface monitors the power supply for overcurrent conditions and shuts down power to the DUT if such conditions are detected.

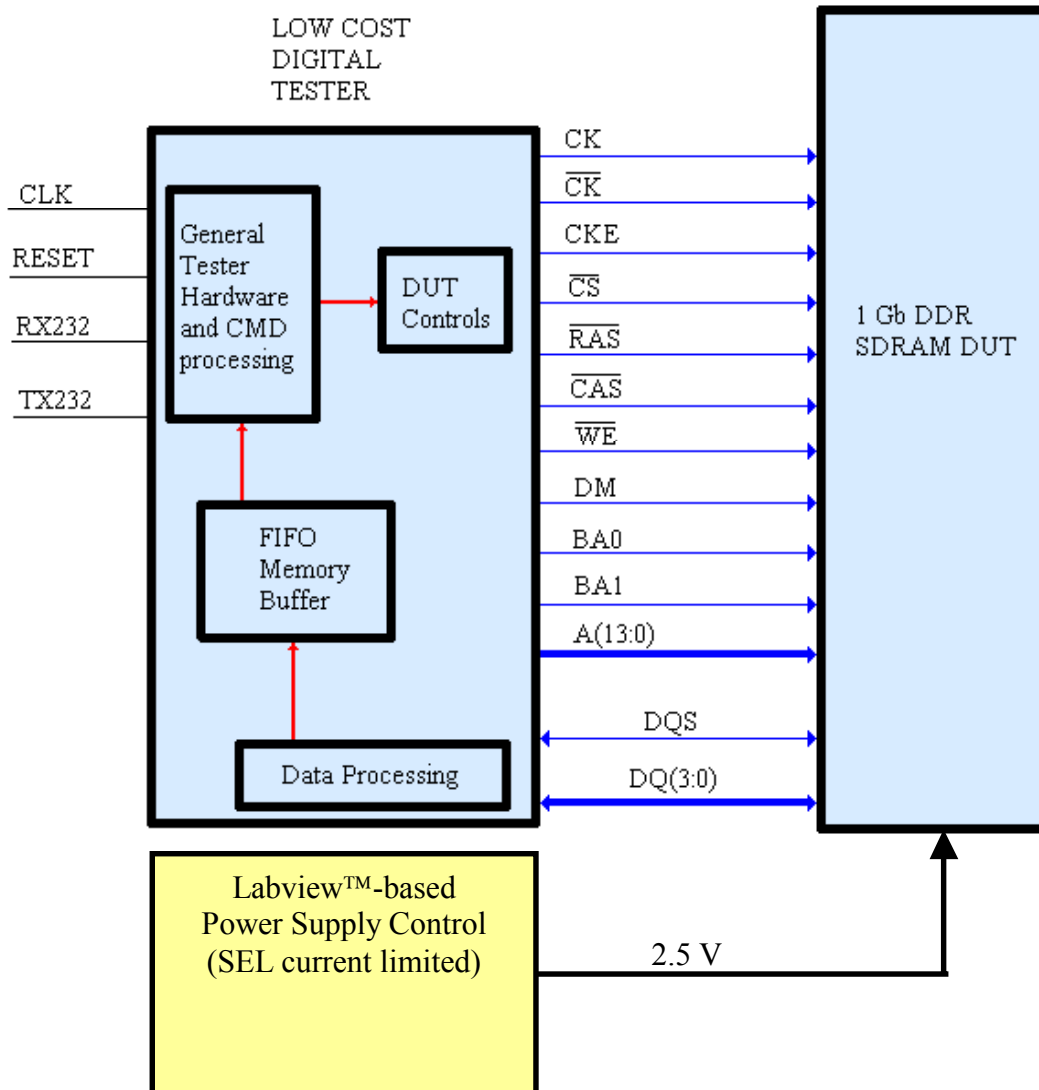


Figure 1. Overall Block Diagram for the testing SDRAMs with the low-cost tester.

V. Results

During testing at SEETF, the KH41G0X38 was irradiated with a single ion, Xenon, but at multiple angles to provide a greater range of incident effective LETs. The DUT was oriented normal to the incident beam, and at 45 and 60 degrees to the normal to yield higher effective LETs (~ 27 - $108 \text{ MeV}\cdot\text{cm}^2/\text{mg}$). SEUs, MBUs and SEFIs were seen for all LETs. SEL was seen only at the highest LET ($\sim 108 \text{ MeV}\cdot\text{cm}^2/\text{mg}$) and with the part heated to 85 degrees C. (Figure 2 shows the SEL cross section at LET $\sim 108 \text{ MeV}\cdot\text{cm}^2/\text{mg}$ and temperature 85 °C, along with upper limits for LET $\sim 46.5 \text{ MeV}\cdot\text{cm}^2/\text{mg}$.) No SEL was seen at room temperature up to an effective LET $\sim 60 \text{ MeV}\cdot\text{cm}^2/\text{mg}$. The SEFI cross section was near saturation over the range of LETs available for this test, while the SEU and MBU cross sections did not saturate. Subsequent testing was undertaken at TAMU to better determine the threshold LET for

these effects. There was some evidence that for low LETs, the cross section may not scale with effective LET. However, the uncertainties in LET estimations for angled ions and the additional beam straggle make it difficult to state this with certainty. Only the normally incident data are shown here. The relatively large SEFI cross section made it difficult to determine SEU cross sections or to pinpoint the fluence where a SEFI occurred. As such, SEFI and SEU and multi-bit upset (MBU) cross sections had to be determined during post-processing of the data. Figure 3 shows the SEU, MBU and SEFI cross sections.

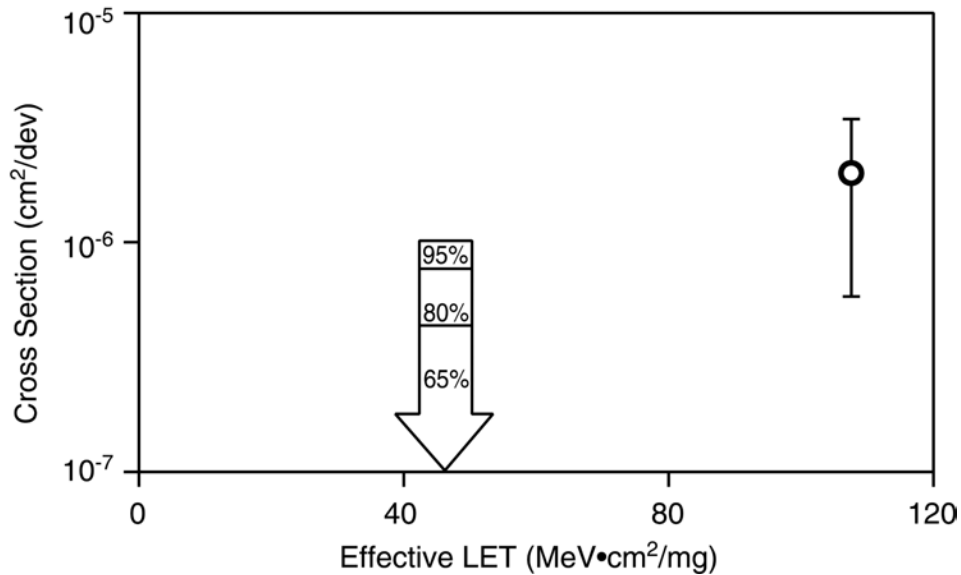


Figure 2 SEL cross section vs. LET (arrow at LET=36 indicates SEL was not observed and indicates the upper limits consistent with the given confidence limits).

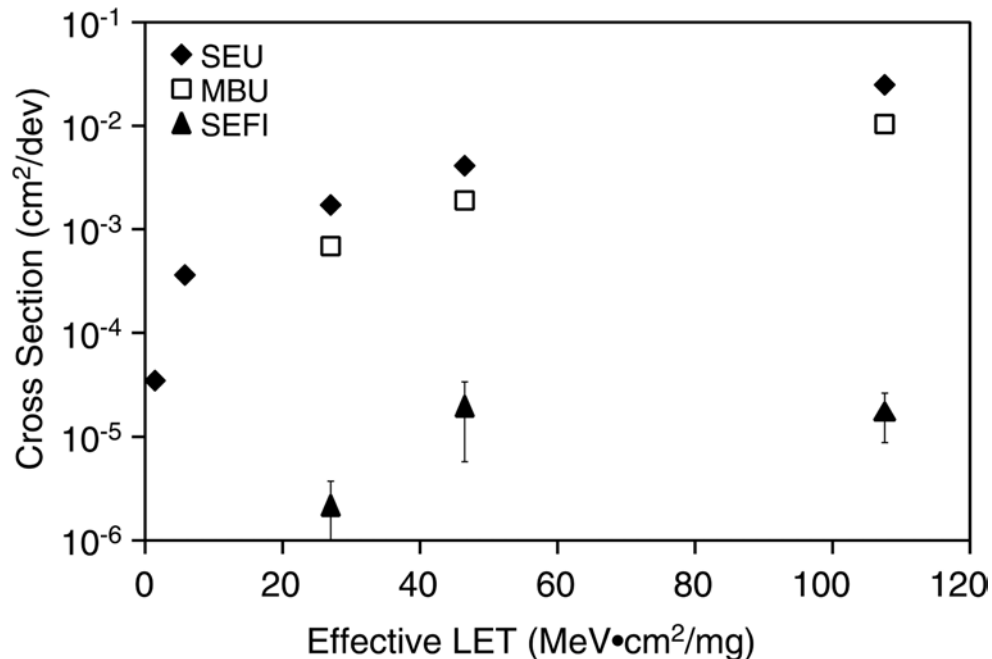


Figure 3 SEU, MBU and SEFI cross sections vs. LET

No obvious incidence of stuck bits was seen either during the run or during post processing.

In looking at figure 3, several features are noteworthy. First, the SEU and MBU cross sections do not saturate at the highest effective LETs in the test, indicating that charge collection by diffusion plays a significant role in these parts for these phenomena. In contrast, the SEFI cross section seems to be saturating. A second point is that the MBU cross section is roughly 50% of the SEU cross section for all LETs used in this test. This may be because the ultra-high energy ion beam tends to create a sufficiently large charge track that angle effects are obscured. This also means that a hamming code would not be effective for these parts, although a modified hamming code (single nibble correct) or Reed-Solomon type code could be. In contrast, no MBUs or SEFIs were seen for low LET.

Proton testing at IUCF with 200 MeV protons yielded a saturated (?) cross section of $\sim 3\text{-}4\text{E-}19\text{ cm}^2$. No significant effect was seen varying the tilt or roll angle of the DUT. Pattern effects are well under a factor of 2--more like 45% of errors were 0 to 1 and 55% were 1 to 0. In proton testing, the DUT remained functional up to a TID of roughly 130 Krad(Si).

VI. Recommendations

In general, devices are categorized based on heavy ion test data into one of the four following categories:

- Category 1: Recommended for usage in all NASA/GSFC spaceflight applications.
 - Category 2: Recommended for usage in NASA/GSFC spaceflight applications, but may require mitigation techniques.
 - Category 3: Recommended for usage in some NASA/GSFC spaceflight applications, but requires extensive mitigation techniques or hard failure recovery mode.
 - Category 4: Not recommended for usage in any NASA/GSFC spaceflight applications.
- Research Test Vehicle: Please contact the P.I. before utilizing this device for spaceflight applications

The Samsung KH41G0X38 2 Gbit NAND Flash memory is a Category 3 device.

VII. Further Test Requirements

This test represents a preliminary characterization of SEE vulnerability of the Samsung KH41G0X38. Additional testing is required before these devices can be considered for space applications. Such testing would involve a better determination of the onset LET for SEL, SEU, MBU and SEFI. While the SEL mode observed did not destroy the part (we did have current limiting), additional testing to ensure all SEL modes are nondestructive and do not result in latent damage is highly desirable. Additional TID testing will be carried out to determine sensitivity to this degradation mode.